

FIG 1

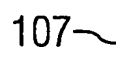


FIG 2

The circuit diagram illustrates a differential signal processing circuit 250. It features a differential pair of PMOS transistors 203 and 204, and a differential pair of NMOS transistors 207 and 208. The PMOS gates are connected to a common gate voltage 212, which is derived from a voltage divider 218, 222 and a feedback network 213, 214. The NMOS gates are connected to a common gate voltage 210, which is derived from a voltage divider 207, 210 and a feedback network 209, 211. The circuit also includes various capacitors (223, 224, 226, 227, 230, 233) and resistors (217, 220, 221, 229, 231, 232, 234) for biasing and signal processing. The output nodes are 201, 205, 215, 217, 208, and 211.

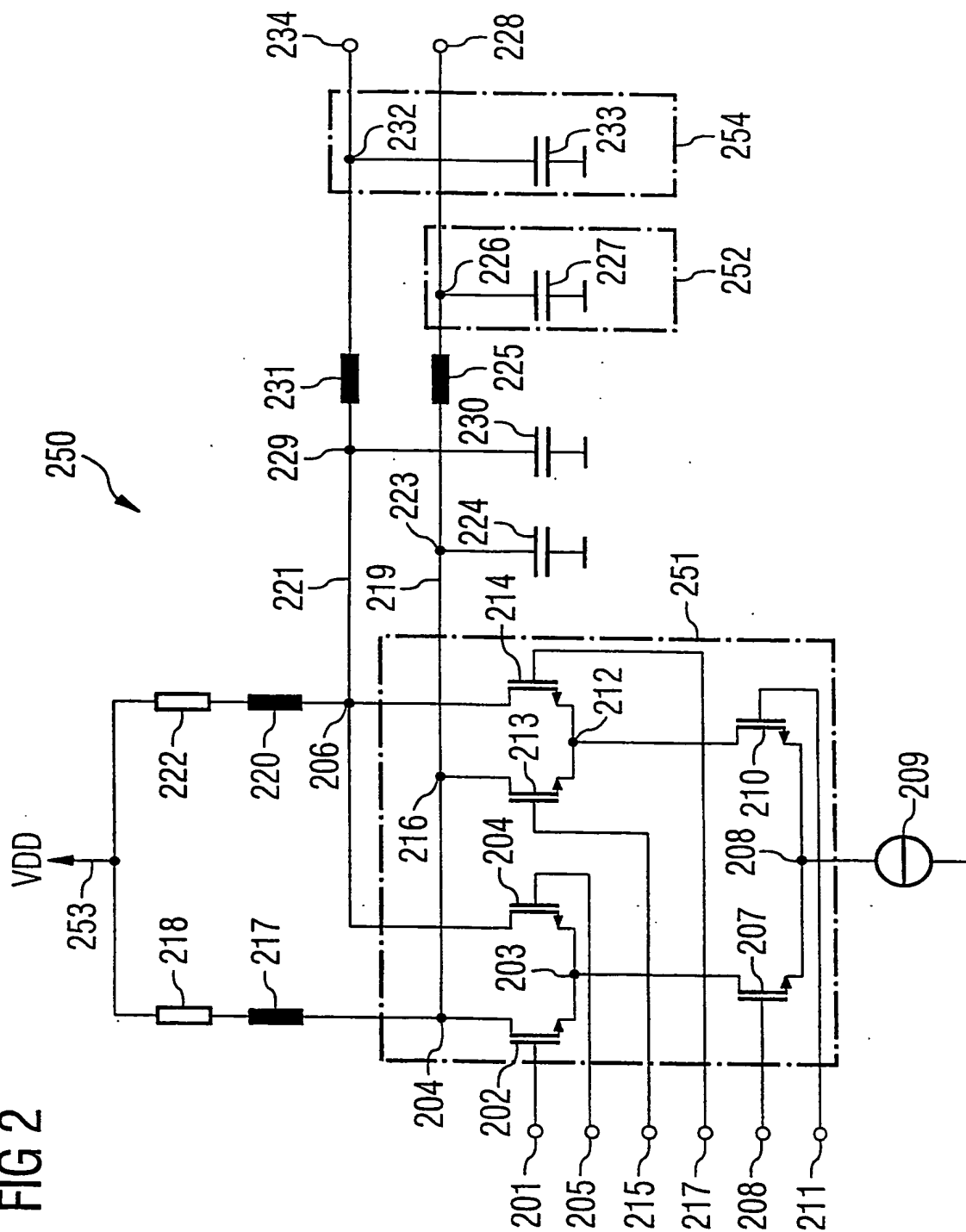


FIG 3

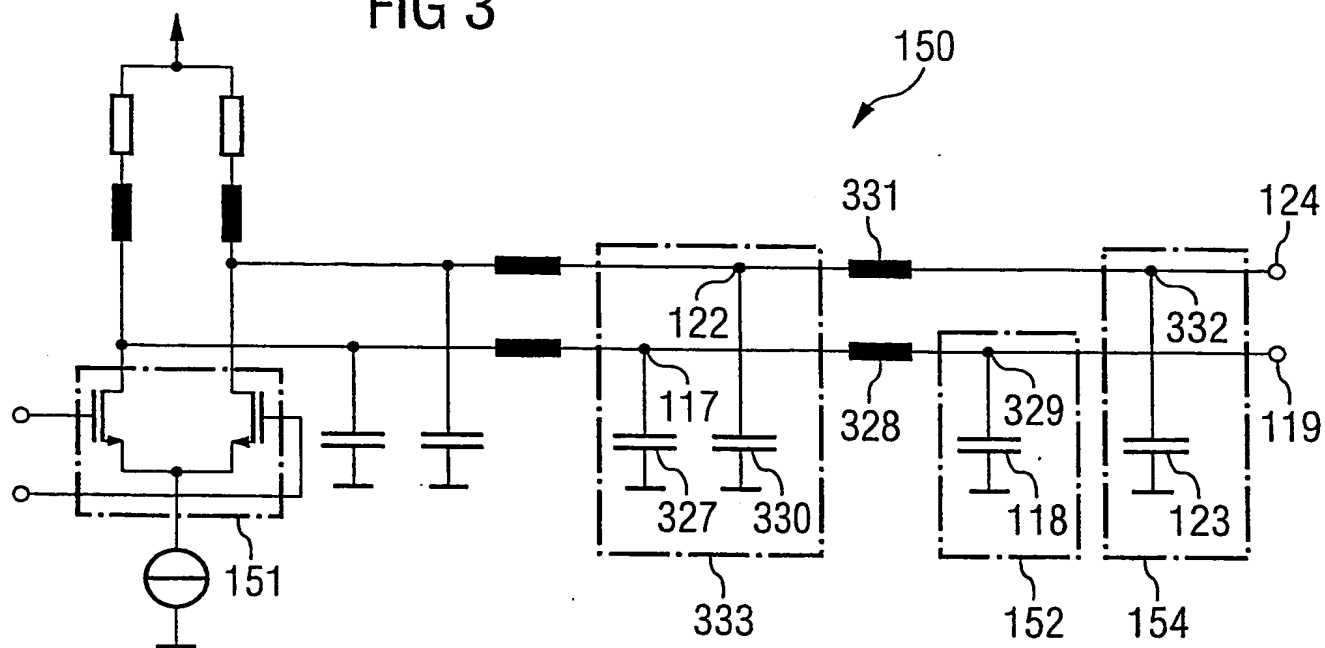


FIG 4

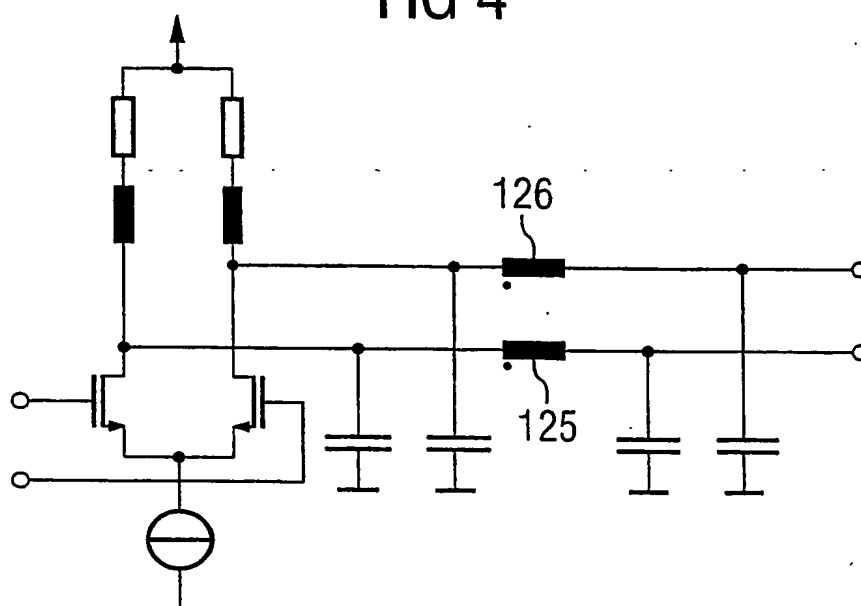


FIG 5

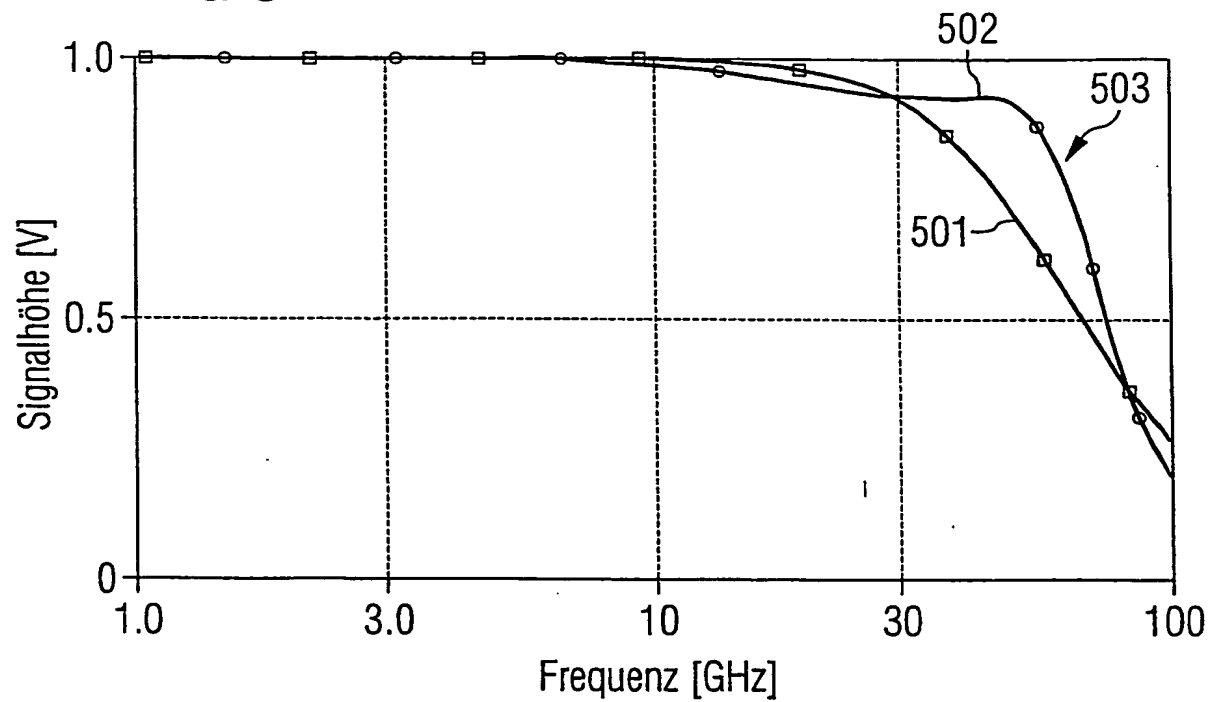


FIG 6A

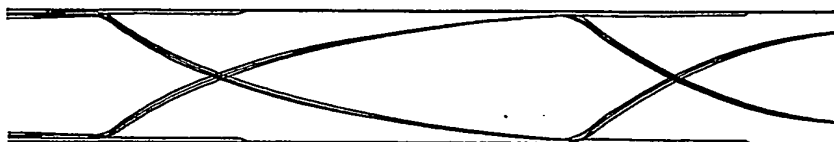


FIG 6B



FIG 6C



The circuit diagram shows a multi-stage CMOS amplifier. The input stage consists of a differential pair of NMOS transistors (2 and 3) with a tail current source (5). The gates of these transistors are connected to a common-mode feedback network (10) that includes PMOS transistors (11 and 14) and NMOS transistors (9 and 12). The output of the first stage is taken differentially from the drains of transistors 2 and 3. This signal is then amplified by two more stages, each consisting of a PMOS load transistor (17 and 23) and an NMOS driver transistor (15 and 21). The final output is taken differentially from the drains of the second stage (19 and 24). The circuit is powered by VDD and ground.